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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,848	06/19/2003	Jonathan B. Ballagh	X-1192 US	7556

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EXAMINER
PIERRE LOUIS, ANDRE

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,848	BALLAGH ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2.0 Claims 1-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Hassoum (U.S. Patent No.6, 487,648), in view of Read et al. (U.S. Patent No. 5,625,580).

2.1 In considering the independent claims 1,8,11,12,13,14, 24, and 27, Hassoum substantially teaches an apparatus for clock stabilization detection for hardware simulation, in particular a digital clock module for receiving an input clock signal and a feedback clock signal and for providing an output clock signal, the digital

clock module configured to lock the feedback clock signal relative to the input clock signal and configured to produce a least common multiple (LCM) clock signal and a lock signal *(fig.1-5 & their description, also col.2 line 14-col.3 line 7)*; a state machine for receiving the lock signal and the LCM clock signal and configured to provide a control signal at least partially responsive to the LCM clock signal and the lock signal *(fig.1-5 & their description, item #302 of fig.3, also col.2 line 14-col.3 line 7)*; and a select circuit for receiving the control signal and the output clock signal and configured to mask application of the output clock signal responsive to the control signal *(fig.1-5 & their description, also col.2 line 14-col.3 line 7 and col.7 line 49-col.11 line 45); the examiner interprets the skewed signal (col.10 lines 14-23) to be a functional equivalence of the locked signal).* Although Hassoum does clearly teaches the term LCM, one ordinary skilled in the art would appreciate the output signal generator as being capable of generating the least common signal. Nevertheless, Read et al. teaches a common signal (col.65 line 47-col.66 line 65), also teaches generating control and feedback signals *(fig.6-10, 32-37 & their description; also col.25 line 29-col.28 line 47 and col.60 line 65-col.66 line 65)*. Read et al. further teaches the test program and test vector of claims 24 and 27 *(see fig.5)*. It would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the teachings of Hassoum with Read et al. for the purpose of accuracy and improvement in hardware modeling and timing behaviour analysis. Read et al further reliability and lower cost (*col.8 line 53-col.9 line 49).*

2.2 As per claim 2, the combined teachings of Hassoum and read et al. teach the buffer coupled to receive the output clock signal and to provide the feedback clock signal, the output clock signal generated responsive to the input clock signal *(see Hassoum fig.4 and 10, also col.7 line 49-col.11 line 45); also see Read et al. figures & their description).*

2.3 With regards to claim 3, the combined teachings of Hassoum and read et al. teach that the feedback clock signal is the LCM clock signal *(see Hassoum fig.3-5, col.7 line 14-col.11 line 45); also see Read et al. figures & their description).*

2.4 Regarding claim 4, the combined teachings of Hassoum and read et al. teach that the digital clock module is disposed in a programmable logic device (PLD), and wherein the PLD comprises a configuration logic block configured with the state machine *(see Hassoum fig.1-5, 10 & their description, also abstract & col.2 line 14-col.3 line 7); also see Read et al. figures & their description).*

2.5 As per claim 5 and 22, the combined teachings of Hassoum and read et al. that the state machine is a register *(see Hassoum fig.1-5 & their description, also col.12 lines 1-57); also see Read et al. figures & their description); also see Read et al. figures & their description).*

2.6 With regards to claim 6, the combined teachings of Hassoum and read et al. that the control signal is configured to cause the select circuit to pass the output clock signal for at least approximate edge coincidence with another output clock signal *(see Hassoum fig.1-5 & their description, also col.49 line 14-col.11 line 45); also see Read et al. figures & their description).*

2.7 Regarding claim 7,9, the combined teachings of Hassoum and read et al. that the state machine comprises an edge detector configured to detect at least proximal phase alignment between the LCM clock signal and the output clock signal to provide the control signal *(see Hassoum fig.1-5 & their description, also col.7 line 49-col.11 line 45; also see Read et al. figures & their description); the examiner interprets the detector in fig.5 of Hassoum to a functional equivalence of the edge detector).*

2.8 As per claim 10, the combined teachings of Hassoum and read et al. that the masking further masks application of the LCM clock signal responsive to the control signal *(Hassoum fig.3-7 & their description, also col.2 line 14-col.3 line 7 and col.17 line 7-32); also see Read et al. figures & their description).*

2.9 With regards to claim 15, the combined teachings of Hassoum and read et al. that the lock is a frequency lock, and wherein the at least proximal 'phase alignment is to a rising edge for all of the plurality of clock signals *(Hassoum fig.3-5 & their description, also col.10 line 38-col.12 line 26); also see Read et al. figures & their description).*

2.10 As per claim 16, the combined teachings of Hassoum and read et al. that the select circuits are multiplexers (*see Hassoum fig.3-5, 10 & their description); also see Read et al. figures & their description).*

2.11 Regarding claim 17, the combined teachings of Hassoum and read et al. that each of the multiplexers have one input terminal coupled to receive the respective one of the plurality of output clock signals and another input terminal coupled to

electrical ground *(see Hassoum fig.3-5, 10 & their description; also col.13 line 7-col.17 line 33); also see Read et al. figures & their description).*

2.12 Regarding claim 18, the combined teachings of Hassoum and read et al. that the digital clock module is part of a field programmable gate array (FPGA) integrated circuit *(see Hassoum fig.1, 3-5 & 10 and their description; also col. 1 line 13-col.3 line 7 and col.17 line 7-32); also see Read et al. figures & their description).*

2.13 With regards to claim 19, the combined teachings of Hassoum and read et al. that the state machine is configured in the FPGA integrated circuit with configurable logic *(see Hassoum abstract, fig.1, 3-5,10 & their description; also col.1 line 13-col.3 line 7); also see Read et al. figures & their description).*

2.14 As per claim 20, the combined teachings of Hassoum and read et al. that the LCM clock signal and feedback clock signal are sent to respective buffers prior to being input to the state machine and the digital clock module, respectively (*see Hassoum fig.1, 3-5,10 & their description; also col.1 line 13-col.3 line 7); also see Read et al. figures & their description).*

2.15 With regards to claim 21, the combined teachings of Hassoum and read et al. that the buffers are multiplexers configured for buffering *(see Hassoum fig.3-5, 10 & their description; also col.1 line 13-col.3 line 7); also see Read et al. figures & their description).*

2.16 Regarding claim 23, the combined teachings of Hassoum and read et al. that the state machine is configured to produce another control signal for adjusting phase, the other control signal provided to the digital clock module for phase adjustment

of at least one of the plurality of output clock signals *(see Hassoum fig.3-5, 10 & their description; also col.1 line 13-col.3 line 7); also see Read et al. figures & their description).*

2.17 With regards to claim 25, the combined teachings of Hassoum and read et al. that selective application of the output clock signal is done for at least approximate edge coincidence with another output clock signal *(see Hassoum fig.3-5, 10 & their description; also col.13 line 7-col.17 line 33); also see Read et al. figures & their description).*

2.18 As per claim 26, the combined teachings of Hassoum and read et al. that selective application of the output clock signal is done for staggered edges with respect to another output clock signal *(see Hassoum fig.3-5, 10 & their description; also col.13 line 7-col.17 line 33); also see Read et al. figures & their description).*

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.1 Kernahan et al. (U.S. Patent No. 6,801,146) teaches a sample and hold circuit including a multiplexer.

3.2 Alvarez et al. (USPG_PUB No. 2003/0091267) teaches a node management architecture for use at an optical switch/node in an optical communications network.

3.3 Paulos et al. (U.S. Patent No. 6,208,671) teaches an asynchronous sample rate converter.

3.4 Parks (U.S. Patent No. 5,535,377) teaches a method and apparatus for low latency synchronization of signals having different clock speeds.

3.5 Hawkins et al. (U.S. Patent No. 5,347,559) teaches an apparatus and method of data transfer between systems using different clocks.

4. Claims 1-27 are rejected and this action is non-final. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 8, 2006

APL

Paul L. Rodriguez
Primary Examiner
Art Unit ~~2125~~ 2123